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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,346	12/09/2003	Fang-Cheng Chen	TS02-1367	3543

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EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,346	CHEN ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *19-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Group I, claims 1-18 in the reply filed on 7/5/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 19-28 are withdrawn from further consideration by the examiner, 37 C.F.R. 1.142(b) as being drawn to a non-elected invention.

Information Disclosure Statement

The information disclosure statement filed on 2/25/04 has been considered.

Oath/Declaration

Oath/Declaration filed on 12/9/03 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4, 6-7, 10-11, 13, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Chidambaram (U.S. Patent Publication No. 2004/0262694).

Referring to figures 1-6G, Chidambaram teaches a method of forming a semiconductor device on a semiconductor substrate, comprising the steps of:

forming a gate dielectric layer (212) on said semiconductor substrate (204);

forming a conductive gate (214) structure on a first area of said gate dielectric layer (212),

forming first insulator spacers (216) on the sides of said conductive gate structure (214) with the procedure used to form said first insulator spacers (216) also removing a second area of said gate dielectric layer, wherein said second area of said gate dielectric layer is not covered by said conductive gate structure or by said first insulator spacers (see figure 2d),

forming a first doped region in an area of said semiconductor substrate not covered by said conductive gate structure of by said first insulator spacers (208/234, see figure 1);

forming a second insulator spacers (238) on the sides of said first insulator spacers; and

forming a second doped region in an area (243) of said semiconductor substrate not covered by said conductive gate structure, not covered by said first insulator spacers, and not covered by said second insulator spacers (see figure 2I).

2. The method of claim 1, wherein said gate dielectric layer is comprised of a layer selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, hafnium oxide, zirconium oxide, aluminum oxide and **silicon oxide** (212, see paragraph# 30).

4. The method of claim 1, wherein the dielectric constant of said gate dielectric layer is greater than 4 (212, see paragraph# 30). It is inherent that the same material would provide the same dielectric constant.

5. The method of claim 1, wherein said conductive gate structure is comprised of doped polysilicon (214, see paragraph# 31).

7. The method of claim 1, wherein said first insulator spacers are comprised of silicon oxide, at a thickness between about 10 to 300 Angstroms (see paragraph# 23, 31, 10nm=100Angstroms).

8. The method of claim 1, wherein said first insulator spacers are comprised of silicon nitride, at a thickness between about 30 to 400 Angstroms(see paragraph# 23, 31, 10nm=100Angstroms).

10. (Original) A method of forming a semiconductor device on a semiconductor substrate featuring a high dielectric constant (high k), gate insulator layer, comprising the steps of:

forming said high k gate insulator layer on said semiconductor substrate;

forming a conductive gate structure overlying a first area of said high k gate insulator layer;

depositing an insulator layer;

performing a dry etch procedure to first define first insulator spacers on the sides of said conductive gate structure via etching of said insulator layer, and then to remove exposed portions of said high gate dielectric layer, wherein said exposed portions of said high k gate insulator layer are portions not covered by said conductive gate structure or by said first insulator spacers;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said conductive gate structure of by said first insulator spacers;

forming second insulator spacers on the sides of said first insulator spacers, and

forming a heavily doped source/drain region in an area of said semiconductor substrate not

covered by said conductive gate structure, not covered by said first insulator spacers, and not covered by said second insulator spacers.

11. The method of claim 10, wherein said high k gate insulator layer is layer selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide, and silicon oxide.

12. (Original) The method of claim 10, wherein the thickness of said high k gate insulator layer is between about 10 to 200 Angstroms.

13. (Original) The method of claim 10, wherein the dielectric constant of said high k gate insulator layer is greater than 4.

14. (Original) The method of claim 10, wherein said conductive structure is comprised of doped polysilicon, at a thickness between about 300 to 3000 Angstroms.

15. (Original) The method of claim 10, wherein said conductive gate structure is comprised of tungsten silicide.

16. (Original) The method of claim 10, wherein said insulator layer is selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

17. (Original) The method of claim 10, wherein the thickness of said insulator layer is between about 30 to 500 Angstroms.

18. (Original) The method of claim 10, wherein procedure used to both define said first insulator spacers on sides of said conductive gate structure, and to remove exposed portions of said high k gate insulator layer, is an anisotropic RIE procedure performed using Ar/CF4 as a selective etchant for said insulator layer and for said high k gate insulator.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 5 8-9, 12, 14-15, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chidambaram (U.S. Patent Publication No. 2004/0262694) as applied to claims 1-2, 4, 6-7, 10-11, 13, 16-17 above in view of Bertrand et al. (U.S. Patent No. 6,841,449) and Komatsu (U.S. Patent Publication No. 2003/0011035).

Chidambaram teaches all of the limitations as described in claimed invention above. However, the reference does not teach the specific thickness of the layer, etching the gate insulation layer and the dielectric layer to form spacer by using Argon and CF4, and forming a gate electrode by using tungsten silicide instead of polysilicon.

Bertrand et al. teaches forming a gate dielectric layer (5) with the thickness of 25-50 Angstroms, forming a gate electrode (6), forming an insulation layer (7) and etching the insulation layer (7) and the dielectric layer (5) by using Argon and CF4 (see col. 2, lines 30-60, figures 1a-1b).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etch the gate insulation layer and the dielectric layer to form spacer by using Argon and CF4 in process of Chidambaram as taught by Bertrand et al. because the process would provide high selective without overetch the bottom layer.

Komatsu teaches forming a gate electrode tungsten silicide (104) with the thickness of about 100nm=1000Angstrom.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made would form a gate electrode by using tungsten silicide (104) with the thickness of about 100nm=1000Angstrom in process of Chidambaram as taught by Komatsu because the process would provide a low-resistance gate electrode, suited for a higher-speed operation of the semiconductor device.

conductive gate structure is comprised of

doped polysilicon (214, see paragraph# 31) at a thickness between about 300 to 3000 Angstroms6. The method of claim 1, wherein said conductive gate structure is comprised of metal silicide such as tungsten silicide.

9 . the method of claim 1, wherein procedure used to define said first insulator spacers on sides of said conductive gate structure, and to remove exposed portions of said gate dielectric layer, is an anisotropic RIE procedure (see paragraph# 23) performed using Ar/CF_4 as a selective etchant for said first insulator spacer and for said gate dielectric layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN